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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/763,858 | 01/21/2004 | Haruki Ito | 9319I-000651 | 9075 |

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| EXAMINER | |
|---|---|
| LEE, CHEUNG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2812 | |

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/763,858 | ITO, HARUKI | |
| | Examiner | Art Unit | |
| | Cheung Lee | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of Group I, claims 1-9, in the reply filed on June 30, 2005 is acknowledged. The traversal is on the ground(s) that all groups of claims are sufficiently related to each other that an undue burden would not placed upon the examiner. This is not found persuasive because Group I (claims 1-9) is drawn to method, and Group II (claims 10-31) is drawn to device. Method and device are classified in two different classes, and two different search areas. Therefore, a burden would be placed examining all groups of claims upon the examiner.

The requirement is still deemed proper and is therefore made FINAL.

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) submitted on January 21, 2004 was filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Specification*

3. The disclosure is objected to because of the inconsistent language: on page 9, line 8, "penetrating space" appears to mean a recess without any limitation on its depth, while on page 10, it makes a distinction to a recess 22, it appears to mean "a hole that goes completely through the resin layer."

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner cannot determine the range for "too fine pattern to be resolved." As best understood, claims 2-4 concern the depth of the recess, deep enough to give enough adhesion but not too deep enough to go through the whole thickness of the resin.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (U.S. Publication 2002/0005568).

6. With respect to claim 1, Kikuchi discloses a method of manufacturing a semiconductor device (page 2, paragraph 30) comprising: forming a resin layer (page 2, paragraph 40; page 5, paragraphs 92-93) on a substrate in which a plurality of

integrated circuits are formed (page 2, paragraph 32; page 5, paragraph 91); forming a recesses in a surface of the resin layer (fig. 5C; page 2, paragraph 40; page 5, paragraphs 92-95); forming an interconnecting line on the resin layer (page 2, paragraph 42; page 6, paragraph 96), to pass along any one of the recesses (page 6, paragraph 96; fig. 10D, item 303); and cutting the semiconductor substrate into a plurality of semiconductor chips (page 2, paragraph 37; page 6, paragraph 100), but Kikuchi does not disclose expressly wherein each of the recesses is formed to have an opening width less than a thickness of the interconnecting line, and to have a depth of at least 1 μm. According to Kikuchi, the protective layer 130 and resin layer 140 have total thickness of 2 μm (page 2, paragraphs 39-40), so the recesses depth in figure10B is at least 1μm. Kikuchi also discloses a recess is formed to improve the adhesion between the interlayer film and the metallic thin film (page 2, paragraph 40). Therefore, the examiner takes the position that the width and the depth of the recess have to be chosen to fulfill this objective while not degrading the characteristics of the insulating layer (resin and protective layers) and vary with the requirements of a specific application. The examiner takes the position that the substrate (page 2, paragraph 31) in the reference is obviously be a semiconductor substrate, since Kikuchi discloses the semiconductor device. Also, the examiner takes the position that the formation of a plurality of recesses is obviously achieved because the single semiconductor device is diced from the entire wafer (page 2, paragraph 37).

7. With respect to claim 5, Kikuchi discloses a method of manufacturing a semiconductor device as set forth in claim 1, further comprising roughening the surface

of the resin layer after forming the recesses (page 2, paragraph 40), but Kikuchi does not disclose expressly wherein roughening the inner surfaces of the recesses, before forming the interconnecting line. Kikuchi discloses the exposed area of the interlayer film can be made larger and roughened (page 2, paragraph 40), the exposed area includes the inner surfaces of the recesses. As a result of this roughening the contact area between the interlayer film and the metallic thin film is greatly enlarged, the roughening is obviously performed before forming the metallic thin film, and this increases the adhesion between the two films (page 2, paragraph 40).

8. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Wolf et al. ("Silicon Processing for the VLSI Era", Vol. 1, Ch. 12, page 407-409; hereinafter "Wolf").

9. With respect to claim 2, Kikuchi discloses a method of manufacturing a semiconductor device as set forth in claim 1, wherein the resin layer is formed the photosensitive resin precursor (page 2, paragraph 40; page 5, paragraph 93), wherein in the steps of forming the recesses, photolithography is applied (page 5, paragraph 93), but Kikuchi does not disclose expressly the use of a mask, and wherein the mask includes a transparent-and-opaque pattern for carrying out light irradiation with too fine pattern for the photosensitive resin precursor to be resolved.

Wolf discloses lithography process using a mask containing clear and opaque features for carrying out light irradiation (page 407, bottom portion and fig. 1).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a mask to perform the lithography as conventionally done to obtain desired patterns.

10. With respect to claims 3 and 4, Kikuchi in view of Wolf discloses a method of manufacturing a semiconductor device as set forth in claim 2. Wolf discloses wherein the photosensitive resin precursor is a negative type including an insoluble light-sensitive portion (page 407 and fig. 1), but Kikuchi in view of Wolf does not disclose expressly wherein the transparent-and-opaque pattern includes an opaque portion having a width less than or equal to the thickness of the interconnecting line (pertaining to claim 3), and wherein the width of the opaque portion is less than or equal to one-fourths of a thickness of the resin layer (pertaining to claim 4). Kikuchi discloses the depth of the trench is not limited but in order to enlarge the contact area it is desirable to etch until just before the protective layer 130 is exposed (page 4, paragraph 64). The opaque portion is to form the recess. The arguments concerning dimensions in claim 1 also apply.

11. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Ma (U.S. Patent 6,713,859).

12. With respect to claim 6, Kikuchi discloses a method of manufacturing a semiconductor device as set forth in claim 5, but Kikuchi does not disclose expressly forming a second resin layer on the resin layer to cover at least a part of the interconnecting line, after forming the interconnecting line and before cutting the semiconductor substrate.

Ma discloses a second resin layer is deposited over the first conductive traces and the first resin layer (col. 6, lines 1-34; fig. 3H, item 338). The individual microelectronic dice cut through the build-up layers, as shown in figure 1M. So, it is obvious that the steps of cutting the substrate (col. 5, lines 46-63) would have been performed after forming second resin layer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a second resin layer on the first resin layer, as taught by Ma. The motivation for doing so would have been to achieve protection of the device against moisture encroachment and delamination, and against any cracking of the semiconductor element.

13. With respect to claim 7, Kikuchi in view of Ma discloses a method of manufacturing a semiconductor device as set forth in claim 6, but Kikuchi does not disclose expressly forming recesses and projections on a surface of the second resin layer. Ma discloses forming recesses and projections (fig. 3I, items 342 and 344) on a surface of the second resin layer (fig 3I, item 338).

14. With respect to claim 8, Kikuchi in view of Ma discloses a method of manufacturing a semiconductor device as set forth in claim 7, but Kikuchi does not disclose expressly forming a third resin layer on the second resin layer. Ma discloses a third resin layer (fig. 3O, item 374) on the second resin layer (fig. 3O, item 338). The motivation concerning about second resin layer formation stated in claim 6 also apply.

15. With respect to claim 9, Kikuchi in view of Ma discloses a method of manufacturing a semiconductor device as set forth in claim 8, but Kikuchi does not

disclose expressly forming recesses and projections on a surface of the third resin layer. Ma discloses forming recesses and projections (fig. 3I, items 342 and 344) on a surface of the second resin layer (fig 3I, item 338), and this process is repeated until a build-up layer is complete, as shown in figure 3O (col. 6, lines 55-67). So, it is inherent that the steps of forming recesses and projections on the third resin layer surface.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

August 31, 2005

HA NGUYEN
PRIMARY EXAMINER